AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

1. **(Currently Amended)** An analyzer for capturing activity on a transmission medium, comprising:

a data input port configured to receive the activity from the transmission medium, wherein the data input port includes signal conversion logic configured to convert a signal type used by the transmission medium to a signal type used by the analyzer and wherein the signal conversion logic is further configured to index at least a portion of the transmission medium activity;

a control port for controlling modes of operation of the analyzer and for accepting user-defined patterns of activity for triggering; [[and]]

replay logic configured to receive the transmission medium activity from the data input port, receive stored activity from a trace buffer, and select one or the other of the transmission medium activity and the stored activity to output to trigger logic, but not both, wherein the trigger logic includes a trigger sequencer that uses a state machine architecture configured to change states and each level of the state machine can enable any or all of the other levels upon exiting the level; and

trace buffer control logic configured to cause activity received by said replay logic to be read from or written to said trace buffer,

wherein said trace buffer is configured to receive at least a portion of the transmission medium activity from said replay logic, store the at least a portion of transmission medium activity, send stored activity to said replay logic, and send stored activity to a data output port for processing or display, and

wherein said trigger logic is configured to compare a pattern of activity received by the replay logic with a first user-defined pattern of activity and to indicate when the comparison results in a match.

2. **(Original)** An analyzer as recited in claim 1 wherein said trace buffer control logic includes logic for overwriting previously stored activity with new activity.

3. **(Original)** An analyzer as recited in claim 1 wherein said trace buffer control logic includes logic for avoiding overwriting previously stored activity with new activity.

4. **(Previously Presented)** An analyzer as recited in claim 1 further comprising selective capture logic adapted to cause the trace buffer control logic to cause activity from the replay logic to be written to the trace buffer only when the activity from said replay logic matches a second user-defined pattern of activity.

5. **(Previously Presented)** An analyzer as recited in claim 4 wherein said selective capture logic is further adapted to cause information about the type of activity from the replay logic that caused the activity to be written to said trace buffer to be incorporated into the activity stored in the trace buffer.

6. **(Previously Presented)** An analyzer as recited in claim 4 further comprising a timestamp counter for creating information about a time of occurrence of each activity event from the replay logic, so that such information may be incorporated into activity stored in said trace buffer,

wherein said trigger logic is adapted to use time counters such that the pattern comparison is based on a relative time of occurrence of an activity event as indicated by the time counters, and

wherein said replay logic uses said stored time-of-occurrence information to control a replay timing.

7. **(Cancelled)**

8. **(Previously Presented)** An analyzer as recited in claim 6 wherein said replay logic uses the stored time-of-occurrence information to control a replay timing.

9. **(Previously Presented)** An analyzer as recited in claim 8 further comprising a replay output port for sending activity from the replay logic to the transmission medium.

10. **(Cancelled)**

11. **(Previously Presented)** An analyzer as recited in claim 1 wherein said trigger logic is adapted to recognize, for comparison purposes, patterns of activity that consist of a single event and patterns of activity that consist of a sequence of events.

12. **(Previously Presented)** An analyzer as recited in claim 1 wherein said trigger logic includes at least one counter for counting a number of occurrences of an activity event as part of the pattern comparison.

13. **(Previously Presented)** An analyzer as recited in claim 1 wherein said trigger logic is adapted to use time counters such that the pattern comparison is based on a relative time of occurrence of an activity event as indicated by the time counters.

14. **(Previously Presented)** An analyzer as recited in claim 13 wherein said replay logic uses a fixed time between events to output the stored activity with the same timing with which the stored activity was initially received at the data input port.

15. **(Previously Presented)** An analyzer as recited in claim 14 further comprising a replay output port for sending the activity from the replay logic to the transmission medium.

16-22. **(Cancelled)**

23. **(Currently Amended)** An analyzer for analyzing activity on a transmission medium, comprising:

(a) a data input port configured to receive the activity from the transmission medium, wherein the data input port includes signal conversion logic configured to convert a signal type used by the transmission medium to a signal type used by the analyzer and wherein the signal

conversion logic is further configured to index at least a portion of the transmission medium activity;

(b) a trace buffer configured to store said received activity;

(c) replay logic configured to replay stored activity in said trace buffer;

(d) a control port configured to permit a user to define a data pattern to be matched in said received activity; and

(e) trigger logic configured to trigger an action based on a match between said data pattern and said replayed activity, wherein said trigger logic is further configured to latch address information of said match to a storage area, wherein said storage area is a FIFO, wherein the trigger logic includes a trigger sequencer that uses a state machine architecture configured to change states, wherein the trigger logic allows a user to program the trigger sequencer to enable different states.

24-26. **(Cancelled)**

27. **(Previously Presented)** An analyzer as recited in claim 23 wherein said replay logic is adapted to terminate a replay function on finding a match.

28. **(Previously Presented)** An analyzer as recited in claim 23 further comprising means for performing additional analysis of said stored activity.

29. **(Previously Presented)** An analyzer as recited in claim 28 wherein said means for performing additional analysis includes means for creating a histogram.

30. **(Previously Presented)** An analyzer as recited in claim 28 wherein said means for performing additional analysis uses the same circuitry as said replay and trigger logic.

31. **(Previously Presented)** An analyzer as recited in claim 28 wherein said means for performing additional analysis includes means for real time protocol monitoring.

32. **(Previously Presented)** An analyzer as recited in claim 28 wherein said means for performing additional analysis includes means for real time statistical analysis.

33. **(Previously Presented)** An analyzer as recited in claim 28 wherein said means for performing additional analysis includes means for traffic generation.

34. **(Previously Presented)** An analyzer as recited in claim 23 wherein said replay logic function is carried out by a computer chip other than a microprocessor.

35. **(Previously Presented)** An analyzer as recited in claim 23 wherein said replay logic is implemented in computer hardware.

36. **(Previously Presented)** An analyzer as recited in claim 23 wherein the analyzer is adapted to use shared hardware to perform real time monitoring, preparation of statistical information, post-capture analysis and to replay the stored activity.

37. **(Currently Amended)** A replay analyzer comprising:

a data input port for receiving data from a transmission medium, wherein the data input port includes means for converting a signal type used by the transmission medium to a signal type used by the analyzer and means for indexing at least a portion of the transmission medium data;

a trace buffer for storing data;

term logic;

at least one event statistic counter;

selective capture logic for determining which data to store in said trace buffer;

replay logic for replaying data stored in said trace buffer;

a trigger adapted to trigger on a match with replayed data;

trigger logic that includes a trigger sequencer that uses a state machine architecture configured to change states and each level of the state machine can enable any and all of the other levels upon exiting the level; and

a timestamp counter.

38. **(Cancelled)**

39. **(Previously Presented)** An analyzer as recited in claim 37 further comprising a timestamp upcounter.

40. **(Previously Presented)** An analyzer as recited in claim 37 further comprising a control port for allowing user control of the analyzer.

41. **(Previously Presented)** An analyzer as recited in claim 37 wherein said replay trigger is adapted to identify specific data values or events.

42. **(Cancelled)**

43. **(Previously Presented)** An analyzer as recited in claim 37 wherein said term logic performs pattern recognition for the analyzer.

44. **(Previously Presented)** An analyzer as recited in claim 37 wherein said at least one event statistic counter is adapted to provide long term statistics regarding types of events that are occurring, each event type being defined by a term.

45. **(Previously Presented)** An analyzer as recited in claim 44 wherein said terms are selected from the group consisting of command packets, addresses, data transfers, and signal assertions.

46. **(Previously Presented)** An analyzer as recited in claim 37 wherein said selective capture logic uses terms from said term logic to capture only incoming activity that matches predefined or user patterns.

47. **(Previously Presented)** An analyzer as recited in claim 37 further comprising a trigger sequencer that is capable of triggering said trigger.

48. **(Previously Presented)** An analyzer as recited in claim 47 wherein said trigger sequencer is adapted to terminate writing to or reading from said trace buffer.

49. **(Previously Presented)** An analyzer as recited in claim 37 wherein the analyzer has a capture mode and a replay mode that are user-selectable.

50. **(Previously Presented)** An analyzer as recited in claim 37 wherein said replay logic permits selection of data flow source and direction.

51. **(Previously Presented)** An analyzer as recited in claim 50 wherein said data flow source and direction may be selected from (i) a flow starting at said data input port, and to said term logic and said trace buffer, or (ii) from said trace buffer to said trigger.

52. **(Previously Presented)** An analyzer as recited in claim 37 further comprising a replay output port.

53. **(Previously Presented)** An analyzer as recited in claim 52 further comprising an output adapter means;

wherein said replay output port and said output adapter meansare in data communication with each other so as to transmit data from the analyzer through said output port and through said output adapter meansto a bus in order to facilitate traffic generation on the bus.

54. **(Previously Presented)** An analyzer as recited in claim 53 wherein activity stored in said trace buffer is used to generate traffic on a bus.

55. **(Previously Presented)** An analyzer as recited in claim 37 further comprising a control port through which a local or remote user can configure analyzer logic.

56. **(Currently Amended)** An analyzer comprising:

a control port adapted to permit user configuration of the analyzer,

a data input port configured to receive a plurality of data channels from a transmission medium, wherein the data input port includes adaptor logic configured to group select ones of the plurality of data channels in dependence on a protocol of the received data;

a trace buffer configured to store data from said data input port;

trace buffer control logic configured to determine which data from said data input port to store in said trace buffer;

replay logic configured to replay data stored in said trace buffer;

term logic configured to match a desired term with replayed data; and

a trigger sequencer configured to use state machine architecture to trigger on an even, wherein the a trigger sequencer uses a state machine architecture configured to change states between 12 levels of state and each level of the state machine can enable any or all of the other levels upon exiting the level and all 12 states can be enabled simultaneously.

57. **(Previously Presented)** An analyzer as recited in claim 56 further comprising a selective capture feature.

58. **(Previously Presented)** An analyzer as recited in claim 56 wherein said term logic is adapted to perform event pattern recognition.

59. **(Previously Presented)** An analyzer as recited in claim 58 wherein said events are selected from the group consisting of high, low, rising edge, falling edge, either edge and dontcare.

60. **(Previously Presented)** An analyzer as recited in claim 56 further comprising selective capture logic.

61. **(Previously Presented)** An analyzer as recited in claim 56 wherein the analyzer has at least one data capture mode selected from the group consisting of state mode, transitional timing mode, and fixed frequency mode.

62. **(Previously Presented)** An analyzer as recited in claim 56 further comprising trigger logic that asserts a trigger signal when data presented to it matches a predefined pattern or sequence.

63. **(Previously Presented)** An analyzer as recited in claim 56 further comprising stop logic.

64. **(Previously Presented)** An analyzer as recited in claim 56 further comprising trigger logic.

65. (**Cancelled)**

66. **(Previously Presented)** An analyzer as recited in claim 56 further comprising an event statistics counter which generates statistical information based on replayed data.

67. **(Previously Presented)** An analyzer as recited in claim 56 wherein said replay logic selects whether data presented to internal functions of the analyzer comes from said trace buffer or from said data input port.

68. **(Previously Presented)** An analyzer as recited in claim 56 wherein said trace buffer control logic includes stop logic, an address controller, and a memory controller.

69. **(Previously Presented)** An analyzer as recited in claim 56 wherein said trace buffer control logic latches an address value of replay data.

70. **(Previously Presented)** An analyzer as recited in claim 69 wherein said address value is latched to a FIFO.

71. **(Previously Presented)** An analyzer as recited in claim 56 wherein the analyzer is adapted to replay traffic using the same timing that the traffic was captured with.

72. **(Previously Presented)** An analyzer as recited in claim 56 wherein the analyzer is adapted to perform decoding, flagging, finding, sorting, statistics and/or filtering operations using triggering and/or counting hardware that are also used for data capture purposes.

73. **(Currently Amended)** An analyzer for capturing activity on a transmission medium, comprising:

a data input port configured to receive the activity in a plurality of channels from the transmission medium, wherein the data input port includes adaptor logic configured to group select ones of the plurality of channels in dependence on a protocol of the received activity;

a control port for controlling modes of operation of the analyzer and for accepting user-defined patterns of activity for triggering; and

replay logic configured to receive the transmission medium activity from the data input port, receive stored activity from a trace buffer, and select one or the other of the transmission medium activity and the stored activity to output to trigger logic, but not both; [[and]]

trace buffer control logic configured to cause activity received by said replay logic to be read from or written to said trace buffer;

selective capture logic adapted to cause the trace buffer control logic to cause activity from the replay logic to be written to the trace buffer only when the activity from said replay logic matches a second user-defined pattern of activity, wherein said selective capture logic is further adapted to cause information about the type of activity from the replay logic that caused the activity to be written to said trace buffer to be incorporated into the activity stored in the trace buffer

a timestamp counter for creating information about a time of occurrence of each activity event from the replay logic, so that such information may be incorporated into activity stored in said trace buffer,

wherein said trigger logic includes time counters for incorporating a relative time of occurrence of an activity event as part of the pattern comparison, and

wherein said replay logic uses said stored time-of-occurrence information to control a replay timing,

wherein said trace buffer is configured to receive at least a portion of the transmission medium activity from said replay logic, store the at least a portion of transmission medium activity, send stored activity to said replay logic, and send stored activity to a data output port for processing or display, and

wherein said trigger logic is configured to compare a pattern of activity received from the replay logic with a first user-defined pattern of activity and to indicate when the comparison results in a match, wherein said trigger logic is adapted to use time counters such that the pattern comparison is based on a relative time of occurrence of an activity event as indicated by the time counters wherein activity events are stored at a fixed frequency, thereby providing a fixed time between events.

74. **(Previously Presented)** An analyzer as recited in claim 73 wherein said trace buffer control logic includes logic for overwriting previously stored activity with new activity.

75. **(Previously Presented)** An analyzer as recited in claim 73 wherein said trace buffer control logic includes logic for avoiding overwriting previously stored activity with new activity.

76. **(Canceled)**

77. **(Canceled)**

78. **(Canceled)**

79. **(Canceled)**

80. **(Currently Amended)** An analyzer as recited in claim [[78]]73 wherein said replay logic uses the stored time-of-occurrence information to control a replay timing.

81. **(Previously Presented)** An analyzer as recited in claim 80 further comprising a replay output port for sending activity from the replay logic to the transmission medium.

82. **(Canceled)**

83. **(Previously Presented)** An analyzer as recited in claim 73 wherein said trigger logic is adapted to recognize, for comparison purposes, patterns of activity that consist of a single event and patterns of activity that consist of a sequence of events.

84. **(Previously Presented)** An analyzer as recited in claim 73 wherein said trigger logic includes at least one counter for counting a number of occurrences of an activity event as part of the pattern comparison.

85. **(Previously Presented)** An analyzer as recited in claim 73 wherein said replay logic uses a fixed time between events to output the stored activity with the same timing with which the stored activity was initially received at the data input port.

86. **(Previously Presented)** An analyzer as recited in claim 85 further comprising a replay output port for sending the activity from the replay logic to the transmission medium.

87. **(Previously Presented)** An analyzer as recited in claim 1, wherein the signal conversion logic is configured to index at least a portion of the transmission medium activity by generating count bits for respective segments of data in the transmission medium activity and sending the transmission medium activity to the replay logic with the generated count bits.

88. **(Previously Presented)** An analyzer as recited in claim 56, wherein the transmission medium is a gigabit bus and wherein the adaptor logic is configured to group select ones of the plurality of data channels such that a coding used by the gigabit bus is decoded by the adaptor logic.